

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/606,283

Confirmation No. 3354

FAX RECEIVED

In re Application of:

APR 05 2006

Noriko SHINOMIYA

Group Art Unit: 2825

OFFICE OF PETITIONS

Filed: June 26, 2003

Examiner: Nghia M. Doan

For: SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING APPARATUS,  
SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING METHOD, SEMICONDUCTOR  
INTEGRATED CIRCUIT MANUFACTURING METHOD, AND READABLE RECORDING  
MEDIA

INFORMATION DISCLOSURE STATEMENT

U.S. Patent and Trademark Office  
Customer Service Window  
Randolph building  
401 Dulany Street  
Alexandria, Virginia 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the U.S. Patent and Trademark Office is hereby directed to the reference listed on the attached Form PTO-1449. The reference was cited in an Office Action mailed March 7, 2006 in the corresponding Japanese Patent Application No. 2003-0185332. A copy of the reference listed on Form PTO-1449 is attached.

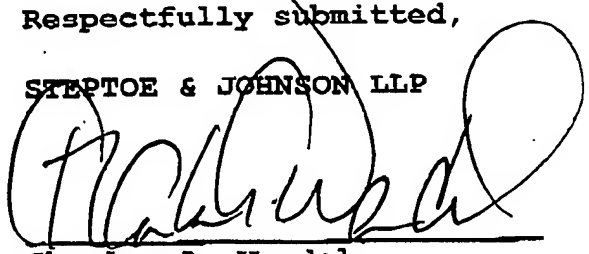
Also attached is applicant's Statement of Relevancy, and an English translation thereof, in which the pertinent paragraphs of the Japanese reference have been translated for the convenience of the Examiner.

Attorney Docket No. 28951.1165

The above information is presented so that the U.S. Patent and Trademark Office may, in the first instance, determine any materiality thereof to the claimed invention. See 37 CFR §1.104(a) and §1.106(b) concerning the USPTO duty to consider and use any such information. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that these references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Respectfully submitted,

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